intel®

AP-506

APPLICATION NOTE

Designing for 80960Cx and 80960Hx Compatibility

Larry Gass
80960 Applications Engineer

With contribution from AP-505
(David Harriman, author)

Intel Corporation
Embedded Processor Division
Mail Stop CH5-233
5000 W. Chandler Blvd.
Chandler, Arizona 85226

March 1995

Order Number: 272556-002

Intel Corporation makes no warranty for the use of its products and assumes no responsibility for any errors which may appear in this document nor does it make a commitment to update the information contained herein.

Intel retains the right to make changes to these specifications at any time, without notice.

Contact your local Intel sales office or your distributor to obtain the latest specifications before placing your product order.

MDS is an ordering code only and is not used as a product name or trademark of Intel Corporation.

Intel Corporation and Intel's FASTPATH are not affiliated with Kinetics, a division of Excelan, Inc. or its FASTPATH trademark or products.

*Other brands and names are the property of their respective owners.

Additional copies of this document or other Intel literature may be obtained from:

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683

CG-041493

CONTENTS

PRODUCT PREVIEW

INTRODUCTION

The 80960HA/HD/HT[1] processors, Intel's new superscalar i960® processor, adds new features and performance to the other well-known products in the i960 processor family. The 80960Hx is designed to satisfy the compute-intensive, data throughput performance requirements of both today's applications and those of the future.

This document addresses the important hardware considerations when designing a "80960Hx ready" system[2]. This is a system which is designed to use an i960 Cx processor[3] and can also use the 80960Hx processor (when available). To help simplify this task, pinout for the 80960Hx PGA package is similar to pinout for the i960 Cx processor PGA package. Although the 80960Hx is not drop-in compatible with all Cx designs, systems can be built with a CPU socket footprint which will accept either processor.

A summary of the most important hardware design considerations are:

power supply — V_{CC} for the Cx is 5V; the Hx uses 3.3V. An 80960Hx-ready system's power supply must accommodate these voltage requirements.

DMA controller — Cx processors have a built-in DMA controller; the Hx does not. An 80960Hx-ready system should not use the Cx built-in DMA controller. Cx pins used for DMA control have different function on the Hx.

byte enable signals — The Hx's byte enable encodings are a superset of the Cx byte enable encodings. The 80960Hx-ready system should be designed to accept all combinations of byte enable encodings.

bus arbitration — The Hx does not grant HOLD requests during an atomic operation (assert HOLDA in response to HOLD), but Cx processors will grant HOLD

Endnotes

1 Throughout this document, "Hx" refers to the i960 HA, HD and HT processors. Information that is specific to each is clearly indicated.

2 "80960Hx-ready" refers to a system designed to use a CA/CF processor that can also use an 80960Hx.

3 Throughout this document, "Cx" refers to both the i960 CA and CF processors. Information that is specific to each is clearly indicated.

PRODUCT PREVIEW

requests after any bus request, including in the middle of atomic accesses. A 80960Hx-ready system must not allow HOLD requests when the external LOCK pin is asserted if semaphore operations are to be performed between bus masters.

The Hx has an additional arbitration signal — BSTALL — which can be used by an external arbiter to indicate the processor has stalled because the bus controller is busy. (The Cx does not have BSTALL.)

external interrupts Interrupt subsystems must produce asynchronous interrupt inputs. The Hx samples interrupts differently than the Cx processors.

N_{XDA} wait states A system must not rely on N_{XDA} wait states between each access. Although both the Hx and Cx processors have programmable N_{XDA} wait states, behavior in the Hx is different. The Hx always inserts N_{XDA} wait states between accesses. The Cx only inserts N_{XDA} wait states between bus "requests." Each bus request can cause multiple bus accesses.

An 80960Hx-ready system must NOT accept data on writes during N_{XDA} wait states. During N_{XDA} wait states, the Hx processor drives the D31:0 bus. Cx processors do not drive valid data during N_{XDA} wait states.

parity The Hx provides built-in byte parity; Cx processors do not. If parity is used when the system contains an Hx processor, pull-up resistors must be provided to ensure that inputs sent to either the processor or to the external parity system do not float.

boundary scan The Hx has an IEEE 1149.1 JTAG interface; conversely, the Cx does not support JTAG. If JTAG is used when the system contains a Cx processor, the processor must be externally bypassed in the JTAG chain.

reserved memory Accesses to reserved memory (0xffxxxxxx) do not appear on the Hx bus. The Cx uses 0xffffffxx to fetch the Initial Boot Record. External decoders should map this memory to two different areas in the processor's address space.

AC timing AC specifications differ for Hx and Cx processors. Of course, AC timing analysis must be performed when designing a 80960Hx-ready system. The Cx AC timings are referenced to PCLK2:1; on the Hx, AC timings are referenced to CLKIN. (The Hx does not have PCLK2:1 signals.)

POWER REQUIREMENTS

The Hx requires a V_{CC} of 3.3V while the Cx operate at 5V. A system can be designed with a socket that accepts either processor. The Hx processor may be damaged if plugged into a socket that supplies 5V V_{CC}. Jumpers, switches, programmable power regulators, or other V_{CC} switching must be provided to select the proper V_{CC} for the processor. The 80960Hx's VOLDET pin can be used to accommodate automatic voltage selection circuitry.

An 80960Hx-ready system requires 5V on the VCC5 pin to provide 5V tolerant inputs.

Providing 3.3 V in a 5 V System

In most system board designs, the 5 V system power supply is routed to the components on the board through a dedicated board layer. With the requirement of a new 3.3 V supply for the Hx, it is not necessary to add a completely new power supply layer to the circuit board, as it is possible to create a 3.3 V "island" around the processor in the existing power supply plane.

Figure 1 shows a recommended "island" layout. The Hx processor's 5 V tolerant input buffers and TTL compatible outputs allow the processor to interface with existing TTL compatible external logic without requiring extra components. Thus, the processor can run at 3.3 V while the system logic runs at 5 V.

Other important considerations are:

- The "island" needs to be large enough to include the processor, the required power supply decoupling capacitance, and the necessary connection to the 3.3 V source.
- To minimize signal degradation, the gap between the 3.3 V "island" and the 5 V plane should be kept small. A typical gap size is about 0.02 inches.
- Minimize the number of traces routed across the power plane gap, since each crossing introduces signal degradation due to the impedance discontinuity that occurs at the gap. For traces that must cross the gap, route them on the side of the board next to the ground plane to reduce or eliminate the signal degradation caused by crossing the gap. If this is not possible, route the trace to cross the gap at a right angle (90 degrees).
- Use liberal decoupling capaciatnce between the 5V plane and the 3.3V island. A 0.01 µf ceramic capacitor every 0.5 to 1.0 inches along the perimeter of the island will greatly reduce the impedance discontinuity.

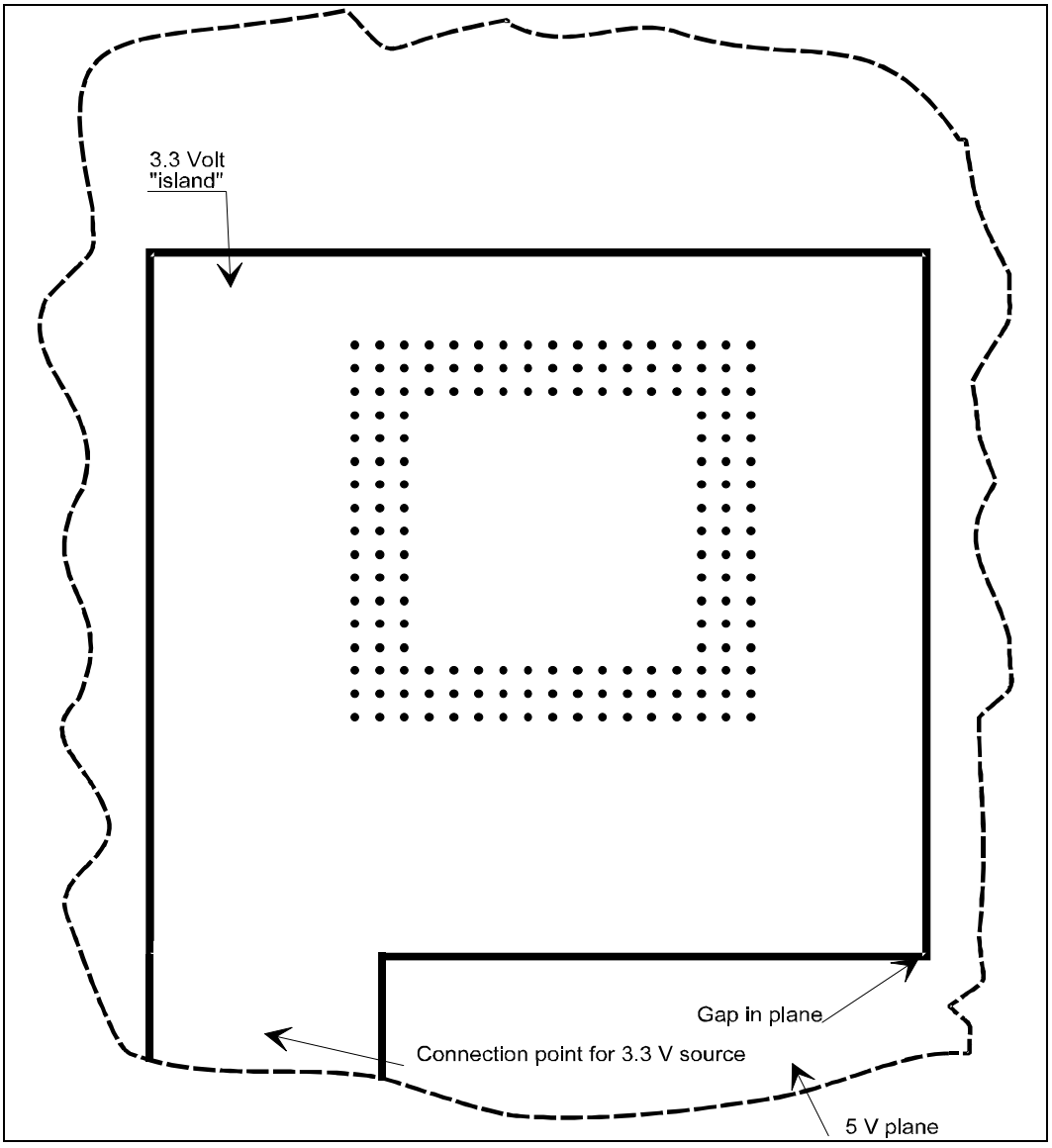

Figure 1. Creating a Power “Island”

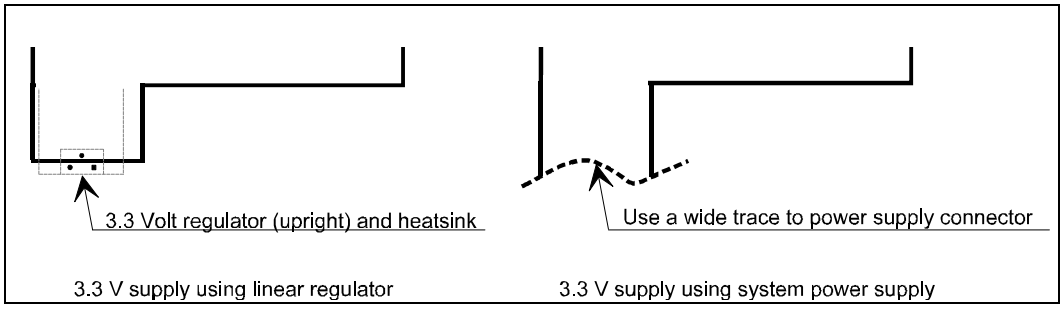

Figure 2. Recommended Power Supply Connection Layout

Choosing a Power Source

The primary concerns which must be addressed when selecting a power source are maximum and minimum load current requirements and response time. The processor power supply must be able to maintain correct voltage regulation at current levels below 10 mA for the Hx in the HALT Mode, and up to the maximum current of 1.5 A.

Executing a HALT instruction causes the Hx to enter the HALT Mode, which causes a significant reduction in the current consumption of the processor in as few as 100 ns. The transition from HALT to the Normal State causes current consumption to return to the normal levels in a similarly short period of time. The processor power supply must be able to maintain correct voltage regulation during these transitions.

There are basically two options for supplying 3.3 V to the processor, either:

- Add a 3.3 V tap to the primary system power supply
- Use on-board secondary regulation to derive 3.3 V from the 5 V system power supply

For on-board secondary regulation, a linear voltage regulator will perform adequately for most designs. If low heat or power dissipation is a design goal, the higher complexity and cost of a switching regulator may be warranted. Switching regulators offer better efficiency, thereby lowering regulator power consumption and heat.

Figure 2 shows recommended layouts for power supply or linear regulator connection to the 3.3 V “island.”

Power Supply Selection For Flexible Systems

Using the 80960Hx's voltage detect sense feature, you may design a flexible system which will automatically provide the proper processor voltage for an 80960Hx or Cx processor. It is also possible to make the selection of processor voltage an option during system board assembly.

VOLDET Automatic Voltage Select Circuit Option

By sampling the VOLDET pin at powerup, system boards can automatically select the processor power supply voltage, enabling a design that may use the 3.3V Hx or a 5 V Cx processor without jumpers or assembly time changes. The VOLDET pin is only present in the PGA package version of the Hx. This pin, which is an NC (No Connect) on the Cx processor, is connected internally to V_{SS} on the Hx. This pin should be left unconnected in designs that do not use the voltage detect feature.

Figure 3 shows an example of VOLDET pin usage with a linear regulator circuit to automatically select the correct power supply voltage. If VOLDET is not connected inside the processor, indicating a 5 V part, the gate of MOSFET Q1 is pulled high, which bypasses the 3.3 V regulator, supplying 5 V directly to the processor. Shorting the regulator's input to the output in this way is harmless for most linear regulators, due to regulator feedback circuitry which shuts the regulator off (contact regulator manufacturers for specifics). Note that in this case, most regulators require Q1 to handle all the processor's current requirements, and so should be a high-current, low on-state-resistance MOSFET. If VOLDET is connected to V_{SS}, indicating a 3.3 V part, the Q1 transistor is turned off, allowing the regulator to function normally. Figure 4 shows a suggested placement and layout for MOSFET Q1.

Other Voltage Selection Options

It is also possible to design a flexible system board where the processor supply voltage is selected by an assembly time option. There are several methods to achieve this; the key requirement being that the design must handle the maximum current of 1.5 A.

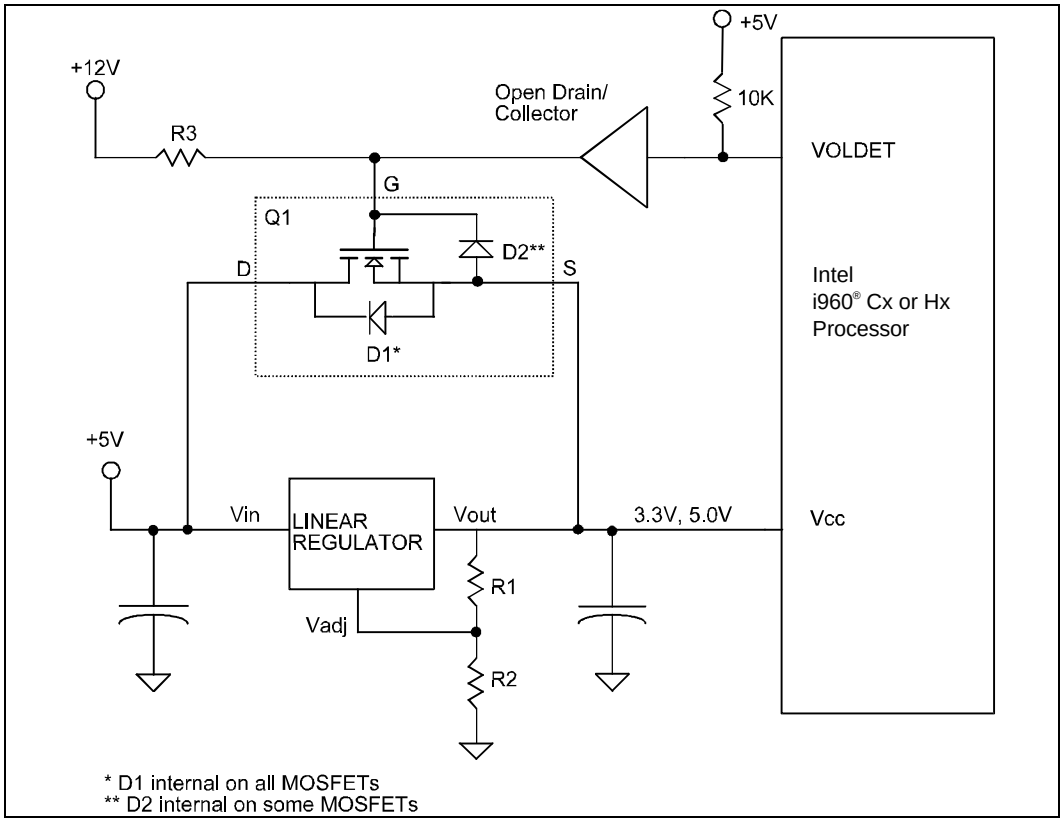

Figure 3. Example Voltage Auto-Select Circuit Topology[4]

Endnotes

[4] Illustration courtesy of Linear Technology Corporation

PRODUCT PREVIEW

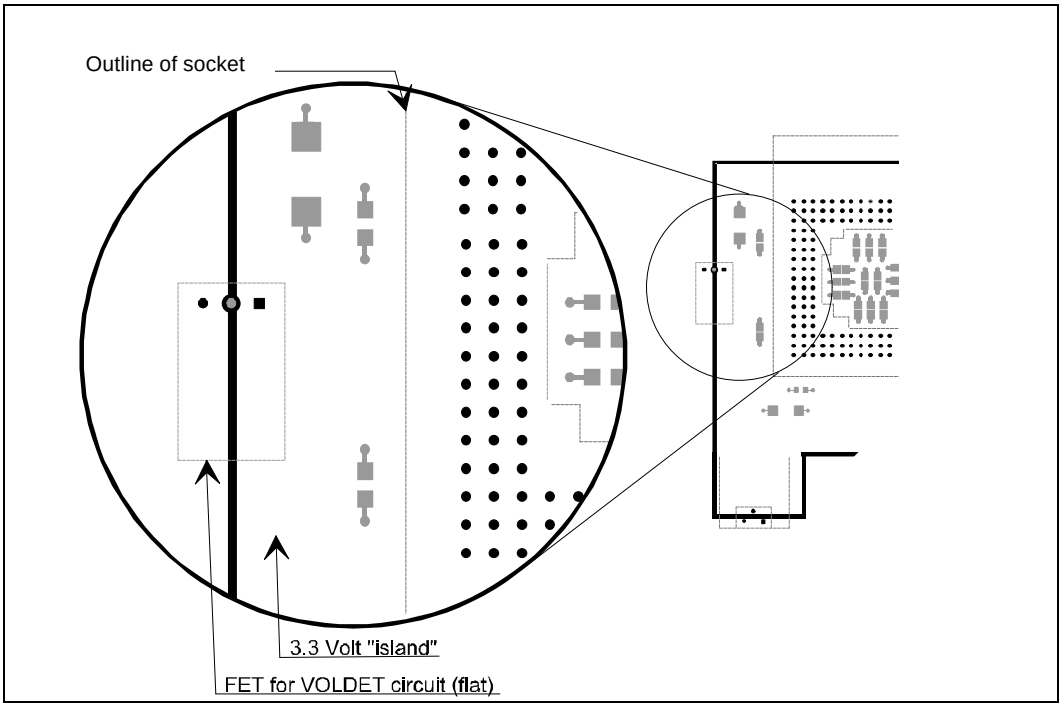

Figure 4. Suggested Placement and Layout for MOSFET Used in Optional Voltage Auto-select Circuit

VCC5 Pin Requirement

For mixed voltage systems where the processor interfaces with 5 V components, the VCC5 pin must be connected to 5 V for proper 5 V tolerant buffer operation. **The VCC5 input should not exceed VCC by more than 2.25 V during power-up, power-down or during operation.** If this requirement is not met, current flow through the pin may exceed 55 mA which may damage the component. To meet this requirement, one of two things must be done:

- The power supply must be designed to turn on and off such that the difference between the VCC5 and VCC voltages never exceeds 2.25 V, or,
- A 100 Ω resistor must be put in series with the VCC5 pin to limit the current through this path (Figure 5 shows a possible layout for this connection).

The 100 Ω series resistor is required for power supplies which do not meet the voltage difference specification, and also provides protection in the case of a power supply failure (where the 5 V supply remains on, but the 3.3 V supply goes to zero).

The VCC5 pin corresponds to a NC (no connect) pin on the Cx processor. This pin has no effect on the operation of the Cx, and can be driven.

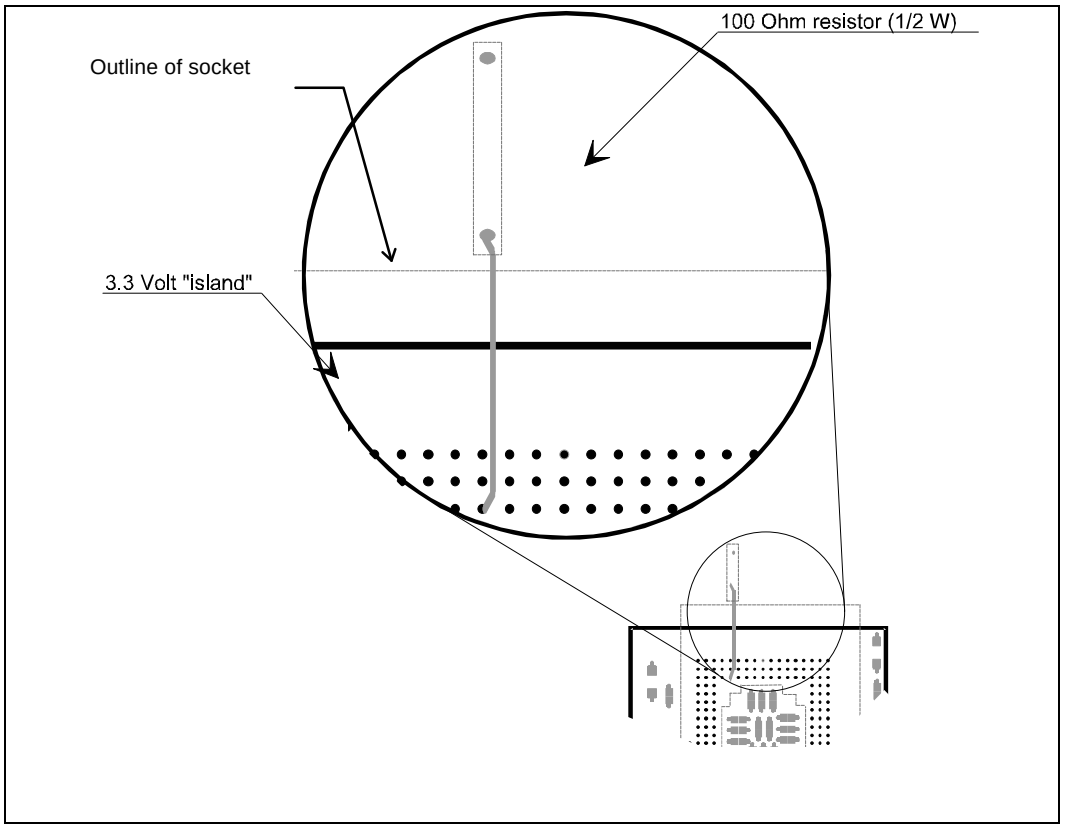

Figure 5. Possible Layout For VCC5 Pin Connection

Processor Power Supply Decoupling

Processor power supply decoupling is critical for reliable operation. With the 80960Hx-ready system, there are two areas of concern, each of which are described in the following subsections:

- High frequency decoupling, necessitated by the processor's high speed operation
- Low frequency decoupling, necessitated by the processor's power saving features

High Frequency Power Supply Decoupling

High frequency decoupling is critical on the Cx processor. It is especially critical on the Hx processor, because of its high speed external bus, and also because of its very fast 66 MHz internal operation.

A reliable design will include a minimum of nine 0.1 μF capacitors and nine 0.01 μF surface mount capacitors between power and ground, evenly distributed, close to the processor. The capacitors must be placed as close to the processor as possible, attached directly to the power and ground planes, or circuit board inductance will significantly reduce their effectiveness.

A typical failure mode caused by inadequate high frequency decoupling is unreliable or inconsistent program behavior. These failures are often intermittent, and are very hard to debug. Figure 6 shows a recommended layout for the high frequency capacitors, with values as shown.

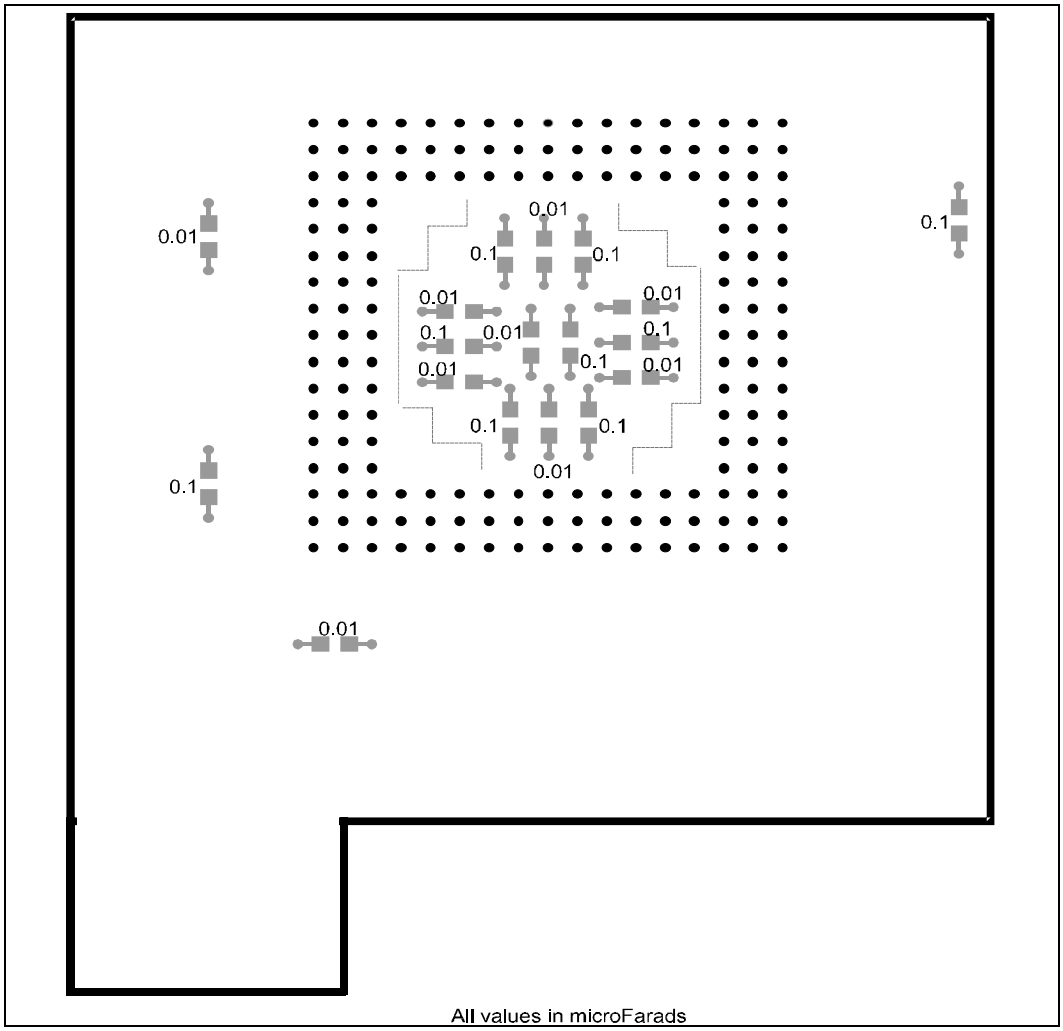

Figure 6. Recommended High-Frequency Capacitor Values and Layout

Bulk Power Supply Decoupling

Bulk, or low frequency, decoupling is needed on all i960 processors, including the Cx and Hx processors, since the Hx processor may switch between normal and low power states very quickly, causing large instantaneous current changes. To properly handle these instantaneous current changes, all designs must have adequate bulk decoupling.

PRODUCT PREVIEW

In 5 V only systems, the processor can use the bulk decoupling capacitance all over the system board; however — with the processor on a separate power plane “island” — it is necessary to place adequate bulk capacitance on the processor “island.” For bulk decoupling, multiple capacitors each in the range of 10 µF to 100 µF are typically used in parallel to achieve the required capacitance while maintaining a low effective series resistance (ESR). You can determine the amount of bulk decoupling required with the following formula:

$$C \approx (\Delta I * \Delta T) / \Delta V$$

where ΔI is the maximum change in current, ΔT is the time it takes the power supply to adjust to the current change, ΔV is the allowable voltage change to remain within specification.

The effective series resistance (ESR) must also be taken into account. You can find the maximum allowable ESR with this formula:

$$ESR \approx \Delta V / \Delta I$$

where ΔV and ΔI are the same as in the first equation.

For example, for the Hx processor, the maximum change in current is about 1.5A. The response time of a linear regulator may be around 15 µs (contact regulator manufacturer for precise value). With no guard band, the maximum allowable supply voltage deviation from 3.3 V is 0.3 V, yielding the following:

$$C \approx (1.5\ A * 15\ \mu s) / 0.3\ V = 75\ \mu F$$

with a maximum allowable ESR:

$$ESR \approx 0.3\ V / 1.5\ A = 0.2\ \Omega$$

Placing four 33 µF tantalum surface mount capacitors in parallel, directly between the power and ground planes, will reduce the ESR below this limit and provide adequate capacitance. Figure 8 shows a recommended layout for this example.

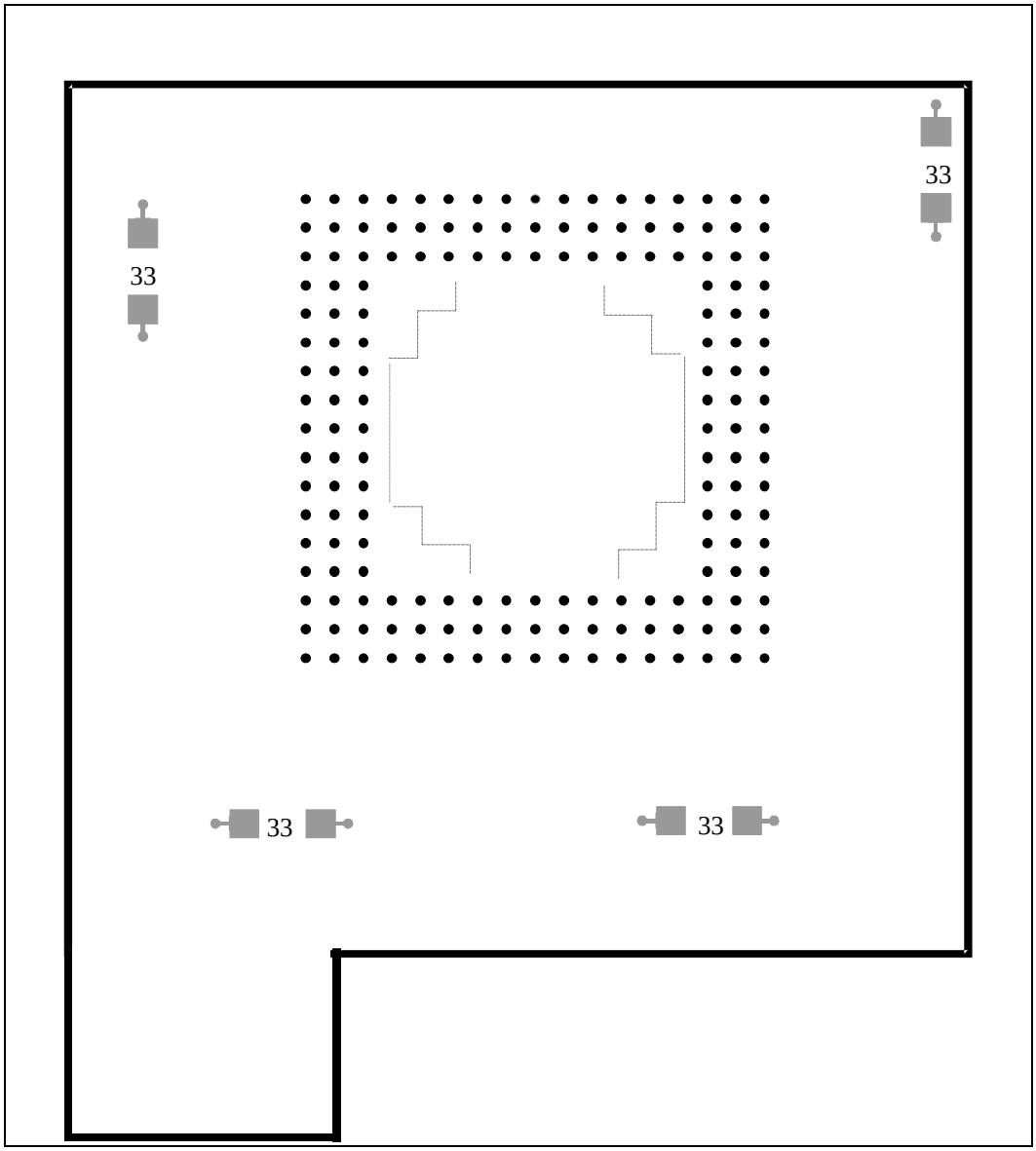

Figure 7. Recommended Bulk Decoupling Capacitor Values and Locations

PRODUCT PREVIEW

BYTE ENABLE SIGNALS

The i960 Cx processors always perform aligned accesses on the bus. This means that the byte enable signals are limited to the following combinations.

Table 1. Byte Enable Signal Combinations

Access	BE3#	BE2#	BE1#	BE0#
WORD	0	0	0	0
SHORT	1	1	0	0
SHORT	0	0	1	1
BYTE	1	1	1	0
BYTE	1	1	0	1
BYTE	1	0	1	1
BYTE	0	1	1	1

In addition to the accesses that the Cx performs, the Hx issues three unaligned cases when accessing 32-bit memory regions.

Table 2. Unaligned Cases When Accessing 32-Bit Memory Regions

Access	BE3#	BE2#	BE1#	BE0#
Unaligned Three-byte	1	0	0	0
Unaligned Three-byte	0	0	0	1
Unaligned SHORT	1	0	0	1

80960Hx-ready systems must be designed to support all encodings. This is accomplished by ensuring that the memory write-enable signals for each byte are dependent on that byte's corresponding BE signal — not on a certain combination of byte enables. When accessing 16- or 8-bit regions, the Hx and Cx processors behave the same.

INTERRUPT SAMPLING

80960Hx-ready systems should be designed to produce asynchronous interrupts to the CPU. Synchronous systems such as lock-step multi-processor systems must meet input setup and hold times on the rising edges of CLKIN for the Hx, and on the falling edges of PCLK2:1 for the Cx. Interrupt pins are sampled on the rising edge of CLKIN for the Hx. Contrarily, on the Cx processors these pins are sampled on the falling edge of CLKIN. The actual sampling of the interrupt pins occurs once every two CLKIN cycles. Improper system behavior occurs if these

setup and hold times are not met in a synchronous system. An example of this is the loosing synchronous operation of multiple processors.

PARITY

A 80960Hx-ready system can implement parity when a Hx is in the CPU socket. Parity is disabled while a Cx is in the CPU socket.

Five parity pins are added to the Hx. Four of these pins, labeled DP3:0, provide byte parity for data and possess the same timing as D31:0. The fifth pin is an output labeled PCHK#. It is asserted if a parity error is detected on reads. PCHK# is asserted in the clock, following the data cycle which has incorrect parity. The Hx DP3:0 pins correspond to the CA/CF‘s "no connect" pins. The Hx PCHK# pin corresponds to the DACK0# pin on the CA/CF. Pull-up resistors are recommended on DP3:0. These resistors are required if parity is not being used to put the Hx parity inputs to a known state. They are also required if parity is being used when a Cx is in the system, in order to provide valid logic levels for the external parity logic. External logic will detect PCHK# high when a Cx processor is in a system. This disables external parity reporting logic.

Parity is only checked on bytes which possess a corresponding active BE signal.

CYCLE TYPE

An 80960Hx-ready system should not use cycle type pins, nor should it use DMA. The Hx uses the pins which correspond to the Cx EOP#/TC# pins for CT3:0. When ADS# is not active, the cycle type is driven to indicate whether it is executing or is in HALT mode. When ADS# is active, CT3:0 indicate the type of bus access currently being started.

Table 3. Bus Access

Cycle Type	ADS#	CT3:0
Program initiated access using 8-bit bus	0	0000
Program initiated access using 16-bit bus	0	0001
Program initiated access using 32-bit bus	0	0010
Event initiated access using 8-bit bus	0	0100
Event initiated access using 16-bit bus	0	0101
Event initiated access using 32-bit bus	0	0110
Reserved	0	0X11
Reserved	0	1XXX
Processor not halted	1	0X0X
Processor not halted	1	0X10
Reserved	1	0011
Processor in HALT mode	1	0111
Reserved for future products	1	1XXX

BSTALL

The BSTALL signal becomes active when the Hx processor can not continue execution until a pending bus transaction is completed. A load instruction followed by an instruction that uses the result of the load, causes a stall until the load is completed. A store or a load instruction, issued when the bus queues are full, also cause a stall. In this case the Hx is stalled until a bus queue entry becomes available. One of these becomes available as a result of processing a pending bus request. The instruction scheduler can cause BSTALL when the processor fetches instructions from external memory. The processor must fetch these instructions due to instruction cache misses.

The BSTALL pin can be used to provide "on demand" bus arbitration. When a system has an external bus master which is given higher priority than the Hx, it can maintain ownership of the bus until the Hx needs the bus. The Hx will assert BREQ when it has a pending bus request. When BREQ is asserted without BSTALL, the processor can continue operation even in the presence of a pending bus request. Some systems may choose to ignore this condition. Alternatively, they don’t give the bus to the Hx, but instead wait until the processor is stalled. The assertion of BSTALL informs the arbitration logic of this condition.

The Cx processor does not have a BSTALL pin — the corresponding pin on the Cx is the DMA# pin. It will be driven high during normal operation (no DMA). This signals a stall condition to the external logic.

If BSTALL is used for bus arbitration in a 80960Hx-ready system, the recommendation is to logically “and” BSTALL and BREQ to indicate when the microprocessor requires the bus. By qualifying BSTALL with BREQ, the resulting signal can be used interchangeably between the Cx and Hx processors. This resulting signal is equivalent to BSTALL on a 80960Hx system, and equivalent to BREQ on a 80960Cx system.

JTAG

If boundary scan is used in an 80960Hx-ready system, a jumper should be used to connect TDI to the next device in the scan chain when a Cx is installed. The jumper should isolate the pin corresponding to TDO from the scan chain.

The Hx supports IEEE 1149.1 boundary scan. This interface consists of 5 pins: 4 input pins and 1 output pin. The JTAG interface utilizes pins used for DMA on the Cx. The Hx JTAG input pins correspond to CA/CF DREQ3:0# input pins. The JTAG output pin corresponds to a Cx DACK1# output pin.

RESERVED MEMORY

The Hx processor is not able to access external memory in the range 0xff000000 to 0xffffffff. This area is reserved for memory mapped registers. Consequently, an Hx processor cannot access the IBR of a Cx system located at 0xffffff00. The IBR of an Hx processor is located at 0xfeffff30 through 0xfeffff5f. It may be beneficial to use a single memory area mapped to two different areas.

For a system to be capable of using memory for either Hx or Cx boot up, at either 0xfexxxxxx or 0xffxxxxxx, address bit 24 should not be used in the boot area decode logic. Using this methodology, the Cx processor accesses this memory using addresses such as 0xffffff00, while the Hx processor uses addresses like 0xfeffff30.

AC TIMING

The timing of signals on the Hx differs from corresponding timing on the Cx. In general, the Hx is faster than the Cx. This generates some interesting design requirements for systems which accept either processor. Specifications for both implementations must be considered — the worst-case numbers must be used in the design.

PRODUCT PREVIEW

The Hx specifications include two values for T_{OV} (output valid delay) corresponding to 5V and 3.3V memory systems. The Hx operates fastest in a 3.3V memory system, one which drives nominally 3.3V as a logic “1”. The processor requires additional time to discharge a 5V “1” data signal down to a valid “0” logic level.

The worst-case sequence for AC timings is reading a “1” (high), then immediately writing a “0” (low). During the write, the processor must discharge the capacitive data bus below 1.5V to produce a valid low. It takes a few nanoseconds longer to discharge a 5V charge than a 3.3V charge.

The Hx specifications described in this section are estimates, and are subject to change when silicon becomes available.

REFERENCE CLOCK

The Cx AC timings for input and output signals are measured against the transitions of the output PCLK2:1 signals. When operating in 1x clock mode, the Cx processor input and output clocks are synchronized. T_{CP}, the CLKIN to PCLK2:1 delay, is +/- 2ns in 1x mode. When operating in 2x mode, the output clock edges are delayed from the input clocks. In 2x mode, T_{CP} is 2 to 25ns at 33 MHz.

The Hx has no output clocks; Hx AC timings are specified according to the input clock.

One of two clocking methods are recommended for a 80960Hx-ready system:

- External logic can be clocked with PCLK2:1 when a Cx is plugged into the socket. It can be clocked with CLKIN when using a Hx processor.

- Always use CLKIN to clock external logic for either a Cx or Hx processor.

For the first of the above recommendations, a method of clock selection must be implemented. Jumpers can be used to select either CLKIN or PCLK2:1 (to route to the synchronous logic within the system). This is a simple methodology because the clocked logic performs the same function with either processor. One benefit derived from this is that the clocks used by external logic are always the processor’s reference clocks.

CLKIN is the reference for the Hx; for the Cx it may be away from the reference (PCLK2:1) by as much as 2ns in 1x clock mode, or 25ns in 2x clock mode. This offset must be considered when analyzing system timing. Due to the wide range of possible delays, it is not practical to use 2x clock mode when using CLKIN for the external logic. The Hx does not support a 2x clock input.

INPUT/OUTPUT TIMING

Input pins specify setup and hold times according to the processor reference clock.

Input signals must be stable between the minimum input setup and hold times. This is the time when the signals are being latched internally within the processor. For minimum input setup and hold values, use the figures with the largest **maximum** values between the two devices.

AC timing parameters for output signals include both a minimum output hold time and a maximum output valid delay. The minimum output hold time specifies the time after a clock during which a signal continues to be valid from the previous state. The maximum output valid delay specifies the maximum time necessary for a signal to switch states.

Output signals switch between the minimum output hold and the maximum output valid times. For minimum output hold, the smallest **minimum** value of the different devices should be used. Maximum output valid delay is the largest **maximum** value of the different devices.

The combined specification for AC timings differs from the sole specification of either a Cx or Hx processor. An application which accepts either a Cx or Hx must operate over this wider range of timing. For example, pins D31:0 are bi-directional and require both input and output timing analysis. The AC timings used in this example are subject to change; refer to current data sheet for actual values.

		D0 (80960CF)	D0 (80960Hx)	Combined
Output timing	TOH (min)	3 ns	1.5 ns	1.5 ns
5V I/O	TOV (max)	16 ns	13 ns	16 ns
3.3V I/O	TOV (max)	na	10 ns	16 ns
Input timing	TIS (min)	3 ns	6 ns	6 ns
	TIH (min)	5	1.5	5

During a write cycle:

- An 80960CF outputs data within a 13 ns window — between 3 and 16 ns after the corresponding clock edge.
- For a 5V I/O system, an 80960 Hx outputs data within a 11.5 ns window — between 1.5 and 13 ns.
- For a 3.3V I/O system, an 80960 Hx outputs data within an 8.5 ns window — between 1.5 and 10 ns.

The combination of these specifications leads to a 14.5 ns window — between 1.5 and 16 ns. Minimum output hold (T_{OH}) analysis must be performed using 1.5 ns. This is the worst case time. Maximum output delay (T_{OV}) analysis must be performed using 16 ns, worst case. Similar "widening" of specifications also occur on input timings.

PINOUT

The following table highlights the differences between the Hx and Cx processors. Differences are indicated with a heavier line around the table cell. Table 4 shows the pin differences between the Cx and Hx. The “comments” section describes recommended usage in an 80960Hx-ready system.

PGA Pin	Hx Signal Name	Cx Signal Name	PGA Pin	Hx Signal Name	Cx Signal Name	PGA Pin	Hx Signal Name	Cx Signal Name	PGA Pin	Hx Signal Name	Cx Signal Name
A1	VSS	NC	**C9**	VSS	VSS	**J15**	VSS	VSS	**Q10**	VSS	VSS
A2	FAIL#	FAIL#	**C10**	VSS	VSS	**J16**	VCC	VCC	**Q11**	VSS	VSS
A3	DP0	NC	**C11**	VSS	VSS	**J17**	A10	A10	**Q12**	SUP#	SUP#
A4	DP2	NC	**C12**	VSS	VSS	**K1**	D13	D13	**Q13**	A30	A30
A5	VOLDET	NC	**C13**	CLKIN	CLKIN	**K2**	VCC	VCC	**Q14**	A28	A28
A6	TRST#	DREQ1#	**C14**	VCC	CLKMODE	**K3**	VSS	VSS	**Q15**	A24	A24
A7	TDI	DREQ3#	**C15**	XINT4#	XINT4#	**K15**	VSS	VSS	**Q16**	A21	A21
A8	TDO	DACK1#	**C16**	XINT6#	XINT6#	**K16**	VCC	VCC	**Q17**	A18	A18
A9	NC	DACK2#	**C17**	XINT7#	XINT7#	**K17**	A11	A11	**R1**	D24	D24
A10	NC	DACK3#	**D1**	D5	D5	**L1**	D15	D15	**R2**	D27	D27
A11	CT0	EOP/TC0#	**D2**	D2	D2	**L2**	D14	D14	**R3**	D31	D31
A12	CT1	EOP/TC1#	**D3**	NC	NC	**L3**	VSS	VSS	**R4**	BTERM#	BTERM#
A13	CT2	EOP/TC2#	**D15**	NMI#	NMI#	**L15**	VSS	VSS	**R5**	HOLD	HOLD
A14	CT3	EOP/TC3#	**D16**	A2	A2	**L16**	A13	A13	**R6**	ADS#	ADS#
A15	XINT1#	XINT1#	**D17**	A3	A3	**L17**	A12	A12	**R7**	VCC	VCC
A16	RESET#	RESET#	**E1**	D7	D7	**M1**	D16	D16	**R8**	VCC	VCC
A17	XINT2#	XINT2#	**E2**	D4	D4	**M2**	VCC	VCC	**R9**	BE0#	BE0#
B1	BOFF#	BOFF#	**E3**	D0	D0	**M3**	VSS	VSS	**R10**	VCC	VCC
B2	STEST	STEST	**E15**	VCC	VCC	**M15**	VSS	VSS	**R11**	VCC	VCC
B3	DP1	NC	**E16**	A4	A4	**M16**	VCC	VCC	**R12**	BSTALL	DMA#
B4	DP3	NC	**E17**	A5	A5	**M17**	A14	A14	**R13**	BREQ	BREQ
B5	TCK	DREQ0#	**F1**	D8	D8	**N1**	D17	D17	**R14**	A29	A29
B6	TMS	DREQ2#	**F2**	D6	D6	**N2**	D18	D18	**R15**	A26	A26
B7	VCC	VCC	**F3**	VCC	VCC	**N3**	VCC	VCC	**R16**	A23	A23
B8	PCHK#	DACK0#	**F15**	VSS	VSS	**N15**	VCC	VCC	**R17**	A22	A22
B9	VCC	VCC	**F16**	VCC	VCC	**N16**	A16	A16	**S1**	D25	D25
B10	VCCPLL	VCCPLL	**F17**	A6	A6	**N17**	A15	A15	**S2**	D29	D29
B11	VCC	VCC	**G1**	D9	D9	**P1**	D19	D19	**S3**	READY#	READY#
B12	VCC	VCC	**G2**	VCC	VCC	**P2**	D20	D20	**S4**	HOLDA	HOLDA
B13	NC	PCLK2	**G3**	VSS	VSS	**P3**	D22	D22	**S5**	BE3#	BE3#
B14	NC	PCLK1	**G15**	VSS	VSS	**P15**	A20	A20	**S6**	BE2#	BE2#
B15	XINT0#	XINT0#	**G16**	A7	A7	**P16**	A19	A19	**S7**	BE1#	BE1#
B16	XINT3#	XINT3#	**G17**	A8	A8	**P17**	A17	A17	**S8**	BLAST#	BLAST#
B17	XINT5#	XINT5#	**H1**	D11	D11	**Q1**	D21	D21	**S9**	DEN#	DEN#
C1	D3	D3	**H2**	D10	D10	**Q2**	D23	D23	**S10**	W/R#	W/R#
C2	D1	D1	**H3**	VSS	VSS	**Q3**	D26	D26	**S11**	DT/R#	DT/R#
C3	ONCE#	ONCE#	**H15**	VSS	VSS	**Q4**	D28	D28	**S12**	WAIT#	WAIT#
C4	VSS	NC	**H16**	VCC	VCC	**Q5**	D30	D30	**S13**	D/C#	D/C#
C5	VCC5	NC	**H17**	A9	A9	**Q6**	VCC	VCC	**S14**	LOCK#	LOCK#
C6	VCC	VCC	**J1**	D12	D12	**Q7**	VSS	VSS	**S15**	A31	A31
C7	VSS	VSS	**J2**	VCC	VCC	**Q8**	VSS	VSS	**S16**	A27	A27
C8	VSS	VSS	**J3**	VSS	VSS	**Q9**	VSS	VSS	**S17**	A25	A25

Table 4. 80960Cx/80960Hx Pin Differences

PRODUCT PREVIEW

Pin	CA/CF	Hx	80960Hx-ready System
A1	NC	VSS	Connect to VSS.
A3	NC	DP0	Should be pulled up with a resistor. In a system with parity, connect to the parity bit which corresponds to D7:0.
A4	NC	DP2	Should be pulled up with a resistor. In a system with parity, connect to the parity bit which corresponds to D23:16.
A5	NC	VOLDET	Can be used to detect which processor is in the socket. High impedance - CA/CF. VSS - Hx
A6	DREQ1#	TRST#	When active (low), causes TAP controller (IEEE 1149.1) to go to Test_Logic_Reset state. This pin should be connected to RESET# through a 10KΩ resisitor.
A7	DREQ3#	TDI	OK to pull-up or drive. If it is driven low, be sure DMA is disabled. If JTAG is used with a Cx in the system, this signal should be connected to TDI of next device in the chain, via a jumper.
A8	DACK1#	TDO	For Cx, this pin will always be high when DMA is not in use. Because this pin is an output, use a jumper or external logic to disconnect this pin when using the Cx.
A9	DACK2#	NC	No connection
A10	DACK3#	NC	No connection
A11-A14	EOP/TC#3:0	CT3:0	Use pull-ups. An output of 1111 indicates a Cx processor is in the system. Indicates the cycle type if ADS# is active. Indicates when the processor is halted if ADS# is not active.
B3	NC	DP1	Should be pulled up with a resistor. In a system with parity, connect to the parity bit which corresponds to D15:8.
B4	NC	DP3	Should be pulled up with a resistor. In a system with parity, connect to the parity bit which corresponds to D31:28.
B5	DREQ0#	TCK	Connect to Test Clock of 1149.1 interface. This pin should be pulled high when not in use.
B6	DREQ2#	TMS	Connect to Test Mode Select of 1149.1 interface. This pin should be pulled high when not in use.
B8	DACK0#	PCHK#	Connect to external parity error recovery/reporting logic. Cx will not generate or check parity.
B13	PCLK2	NC	OK to drive Hx with CLKIN for compatibility.

B14	PCLK1	NC	OK to drive Hx with CLKIN for compatibility.
C4	NC	V_{SS}	Connect to V_{SS}.
C5	NC	VCC5	Connect to 5V through a 100 Ohm resistor if inputs can be driven from 5V logic. Connect directly to 3.3V if inputs are not driven by 5V logic.
C14	CLKMODE	VCC	Connect to processor's V_{CC}.
R12	DMA#	BSTALL	Can use for arbitration.

DESIGN GUIDELINE SUMMARY

A system can be designed which accepts either a Hx or Cx processor. The following items summarize the guidelines discussed in this paper:

- Don't use the DMA controller on the Cx processor
- Isolate V_{CC} for the CPU. Hx = 3.3V; Cx = 5V
- Provide 5V reference voltage for Hx (VCC5)
- Use CLKIN for system timing
- Combine AC specifications for timing analysis
- Accommodate new BE3:0# encodings
- Use pull-up resistors on parity signals
- Connect additional V_{ss} signals
- If using JTAG boundary scan, bypass Cx in the JTAG chain

PRODUCT PREVIEW

REVISION HISTORY

Changes from Rev 001 to Rev 002 include:

Section	Description
AC TIMING	Two paragraphs added after the first: The Hx specifications include two values for T_{OV} (output valid delay) corresponding to 5V and 3.3V memory systems. The Hx operates fastest in a 3.3V memory system, one which drives nominally 3.3V as a logic "1". The processor requires additional time to discharge a 5V "1" data signal down to a valid "0" logic level. The worst-case sequence for AC timings is reading a "1" (high), then immediately writing a "0" (low). During the write, the processor must discharge the capacitive data bus below 1.5V to produce a valid low. It takes a few nanoseconds longer to discharge a 5V charge than a 3.3V charge.
INPUT/OUTPUT TIMING	The second bulleted item in this section changed. WAS: • A Hx outputs data within a 7 ns window — between 1.5 and 8.5 ns. IS: • For a 5V I/O system, an 80960 Hx outputs data within a 11.5 ns window — between 1.5 and 13 ns. • For a 3.3V I/O system, an 80960 Hx outputs data within an 8.5 ns window — between 1.5 and 10 ns.
INPUT/OUTPUT TIMING	Numbers changed in the table that compares Input/Output timing of the Hx and Cx. Output Timing TOV (max) for the Hx (3.3V) changed from 8.5ns to 10ns. Output Time TOV (max) for the Hx (5V) was added (13ns). Input timing for TIS(min) for the Hx changed from 5ns to 6ns. Input timing for TIS(min) for the "Combined" changed from 5ns to 6ns.
Table 4. 80960Cx/80960Hx Pin Differences	Pin definition for A6, last sentence, changed. WAS: This pin should be pulled high when not in use. IS: This pin should be connected to RESET# through a 10KΩ resisitor.